REMARKS

Claims 1-17 are pending in the present application. Claims 1, 6-18, and 20 are rejected. Claims 2-5 are allowable if re-written in independent form including the limitations of any intervening claims. Claims 9 and 17 are objected to as lacking antecedent basis for the term "caposer".

Claims 9 and 17 are amended to replace the term "caposer" with the term "interposer" (see paragraph 0013, first sentence). Because the amendments to Claims 9 and 17 merely correct an obvious clerical error by substituting an equivalent term that provides proper antecedent basis, these amendments are not narrowing. No new matter is added.

Claims 18 and 20 are cancelled. Therefore, the rejection of these claims is moot.

Claim Rejections under 35 USC 102(e)

Claims 1, 6-10, 12-18, and 20 are rejected as being anticipated by Yamagishi et al (U.S. 2004/0239349, hereinafter Yamagishi). The Examiner therefore argues that Yamagishi teaches every element of every claim, either expressly or by implication. (MPEP 706.02(IV) provides the following summary of the relevant standard: "For anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.") Applicant respectfully disagrees.

The Office Action equates Yamagishi's "core layer" 12 (see Fig. 4) with Applicant's claimed "integrated circuit package". Clearly, Yamagishi's core layer 12 is not an integrated circuit package. As is well known in the art, an integrated circuit package is a physical structure that encloses an integrated circuit and provides contact between the integrated circuit and the external environment. Yamagishi's core layer 12 is merely a layer in a printed circuit board ("probe card"), and not an integrated circuit package. Applicant's Claim 1 recites:

> an interposer disposed in the integrated circuit package between the integrated circuit and the inside surface of the integrated circuit package

thereby making it clear that the integrated circuit and the interposer are disposed within the integrated circuit package. Therefore, it is clearly incorrect to equate Yamagishi's core layer 12 with Applicant's integrated circuit package.

Therefore, and for at least these reasons, Claim 1 is allowable over Yamagishi. Claims 6-10 and 12-14 are allowable for at least the reasons of Claim 1, from which they depend.

Claim 15 recites the limitation "the interposer being disposed inside an integrated circuit package between the integrated circuit die and an inside surface of the integrated circuit package". Yamagishi's core layer 12 is again erroneously identified as a integrated circuit package. However, Yamagishi clearly neither teaches nor suggests an interposer and an integrated circuit being disposed together inside an integrated circuit package. The cited paragraphs of Yamagishi, 0042 and 0043, certainly do not disclose this limitation. Therefore, Claim 15 is allowable over Yamagishi. Claims 16-17 are also allowable for at least the reasons of Claim 15, from which they depend.

Claims 18 and 20 are cancelled. Therefore, the rejection of these claims is moot.

Claim Rejections under 35 USC 103(a)

Claim 11 is rejected under 35 USC 103(a) as being unpatentable over Yamagishi. However, Claim 11 depends from Claim 1, and therefore includes the limitation that the "interposer [is] disposed in the integrated circuit package between the integrated circuit and the inside surface of the integrated circuit package". Because Yamagishi's "core layer" 12 is clearly not an integrated circuit package, Yamagishi clearly does not disclose this structure. Therefore, Claim 11 is allowable for at least the reasons of Claim 1.

Allowable Subject Matter

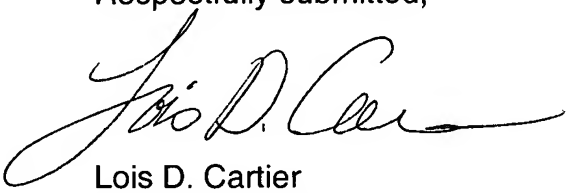
Applicant acknowledges that Claims 2-5 are deemed allowable if properly rewritten as independent claims. However, Applicant believes that all remaining claims are allowable, for at least the reasons described above.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's agent can be reached at Tel: 720-652-3733 (Mountain Time).

Respectfully submitted,



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*I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on July 17, 2006.*

Pat Tompkins
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